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INTERNATIONAL STANDARD

Piezoelectric, dielectric and electrostatic oscillators of assessed quality – Part 1: Generic specification

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PIEZOELECTRIC, DIELECTRIC AND ELECTROSTATIC OSCILLATORS OF ASSESSED QUALITY –

Part 1: Generic specification

FOREWORD

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International Standard IEC 60679-1 has been prepared by IEC technical committee TC 49: Piezoelectric, dielectric and electrostatic devices and associated materials for frequency control, selection and detection.

This fourth edition cancels and replaces the third edition published in 2007. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) the title has been changed;
b) additional matters related to oscillator using SAW or MEMS resonator in "Terms, definitions and general information" have been included;
c) measurement methods of IEC 60679-1:2007 have been removed (they will be moved to IEC 62884 series);

d) the content of Annex A has been extended;

e) a new term and definition DIXO (Digital interfaced Crystal Oscillator) has been added;

f) a new term and definition SSXO (Spread Spectrum Crystal Oscillator) has been added;

g) Annex D has been added.

The text of this standard is based on the following documents:

FDIS	Report on voting
49/1229/FDIS	49/1233/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts of the IEC 60679 series, published under the general title *piezoelectric, dielectric and electrostatic oscillators of assessed quality* can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

PIEZOELECTRIC, DIELECTRIC AND ELECTROSTATIC OSCILLATORS OF ASSESSED QUALITY –

Part 1: Generic specification

1 Scope

This part of IEC 60679 specifies general requirements for piezoelectric, dielectric and electrostatic oscillators, including Dielectric Resonator Oscillators (DRO) and oscillators using FBAR (hereinafter referred to as "Oscillator"), of assessed quality using either capability approval or qualification approval procedures.

NOTE Dielectric Resonator Oscillators (DRO) and oscillators using FBAR are under consideration.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60027 (all parts), *Letter symbols to be used in electrical technology*

IEC 60050-561, *International electrotecnical vocabulary – Part 561: Piezoelectric, dielectric and electrostatic devices and associated materials for frequency control, selection and detection.* Available at www.electropedia.org

IEC 60469, *Transitions, pulses and related waveforms – Terms, definitions and algorithms*

IEC 60617, *Graphical symbols for diagrams.* Available at http://std.iec.ch/iec60617

IEC 60748-2, *Semiconductor devices – Integrated circuits – Part 2: Digital integrated circuits*

IEC 60749-26, *Semiconductor devices – Mechanical and climatic test methods – Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)*

IEC 60749-27, *Semiconductor devices – Mechanical and climatic test methods – Part 27: Electrostatic discharge (ESD) sensitivity testing – Machine model (MM)*

IEC TR 61000-4-1, *Electromagnetic compatibility (EMC) – Part 4-1: Testing and measurement techniques – Overview of the IEC 61000-4 series*

IEC 61340-5-1, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

IEC 62884-1:2017, *Measurement techniques of piezoelectric, dielectric, and electrostatic oscillators – Part 1: Basic methods for the measurement*

ISO 80000-1, *Quantities and units – Part 1: General*

Where any discrepancies occur for any reason, documents shall rank in the following order of precedence:

- detail specification;
- sectional specification;
- generic specification;
- any other international documents (for example of the IEC) to which reference is made.

The same order of precedence shall apply to equivalent national documents.

3 Terms, definitions and general information

3.1 General

Units, graphical symbols, letter symbols and terminology shall, wherever possible, be taken from the following standards:

- IEC 60027;
- IEC 60050-561;
- IEC 60469;
- IEC 60617;
- ISO 80000-1.

3.2 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.2.1
simple packaged crystal oscillator
SPXO
crystal controlled oscillator having no means of temperature control or compensation, exhibiting a frequency/temperature characteristic determined substantially by the quartz crystal resonator employed

[SOURCE: IEC 60050-561:2014, 561-03-30]

3.2.2
overtone crystal controlled oscillator
oscillator designed to operate with the controlling piezoelectric resonator functioning in a specified mechanical overtone order of vibration

[SOURCE: IEC 60050-561:2014, 561-03-20, modified – The word "functioning" has been added.]

3.2.3
crystal cut
orientation of the crystal element with respect to the crystallographic axes of the crystal

Note 1 to entry: It can be desirable to specify the cut (and hence the general form of the frequency/temperature performance) of a crystal unit used in an oscillator application. The choice of the crystal cut will imply certain attributes of the oscillator which may not otherwise appear in the detail specification.

[SOURCE: IEC 60050-561:2014, 561-03-04]

3.2.4
voltage controlled crystal oscillator
VCXO
crystal controlled oscillator, the frequency of which can be deviated or modulated according to a specific relation, through application of a control voltage

[SOURCE: IEC 60050-561:2014, 561-03-41]

3.2.5
temperature compensated crystal oscillator
TCXO
crystal controlled oscillator whose frequency deviation due to temperature is reduced by means of a compensation system, incorporated in the device

[SOURCE: IEC 60050-561:2014, 561-03-36]

3.2.6
oven controlled crystal oscillator
OCXO
crystal controlled oscillator in which at least the piezoelectric resonator is temperature controlled

Note 1 to entry: This mode of operation ensures that the oscillator frequency will remain sensibly constant over the operating temperature range of the OCXO, therefore independent of the frequency/temperature characteristic of the crystal unit.

[SOURCE: IEC 60050-561:2014, 561-03-19, modified – The note to entry has been added.]

3.2.7
surface acoustic wave
SAW
acoustic wave, propagating along the surface of an elastic substrate, the amplitude of which decays exponentially with substrate depth

[SOURCE: IEC 60050-561:2014, 561-01-86]

3.2.8
SAWR
surface acoustic wave resonator
SAW resonator
resonator using multiple reflections of surface acoustic waves

[SOURCE: IEC 60050-561:2014, 561-01-87, modified – The term "SAW resonator" has been added.]

3.2.9
one-port SAW resonator
SAW resonator having a pair of terminals

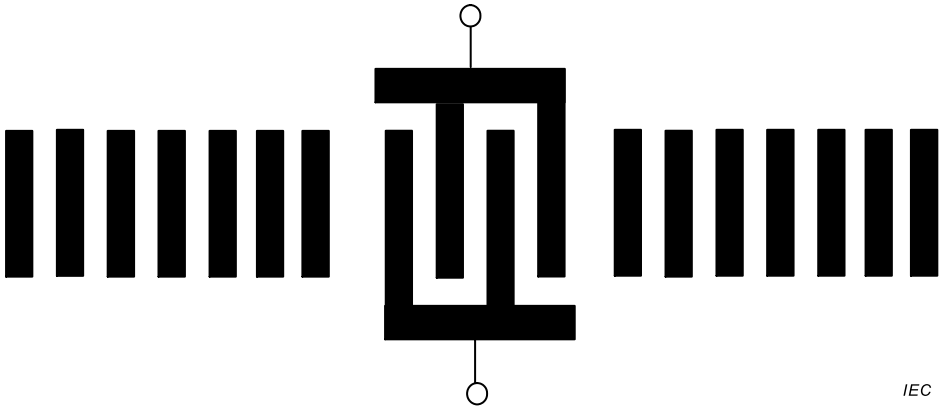
SEE: Figure 1a.

[SOURCE: IEC 60050-561:2014, 561-01-57, modified – The figure reference has been changed.]

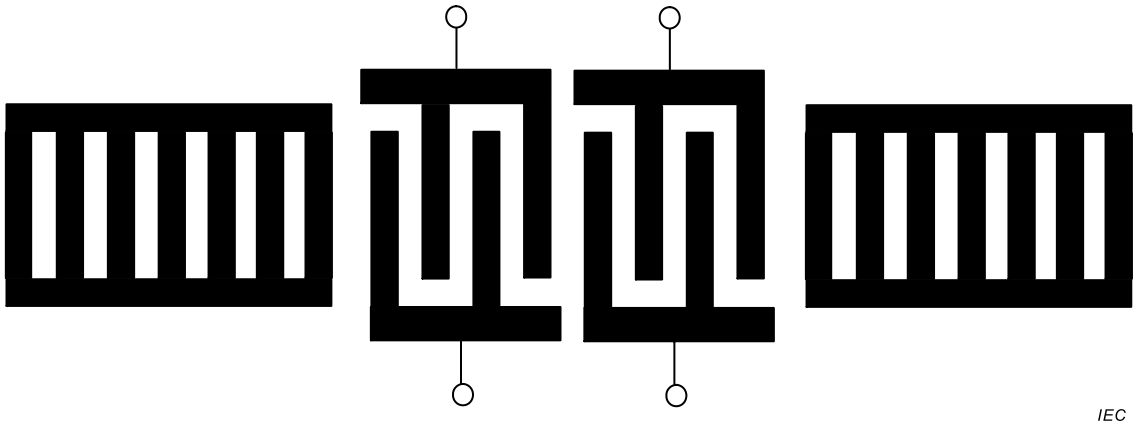
3.2.10
two-port SAW resonator
SAW resonator having input and output ports

SEE: Figure 1b

[SOURCE: IEC 60050-561:2014, 561-01-94, modified – The figure reference has been changed.]



a) One-port resonator with opened array



b) Two-port resonator with shorted arrays

Figure 1 – Basic configurations of SAW resonators

3.2.11
SAW oscillator
oscillator that uses a SAW resonator as the main frequency controlling element

3.2.12
simple packaged SAW oscillator
SPSO
SAW oscillator having no means of temperature control or compensation, exhibiting a frequency/temperature characteristic determined substantially by SAW resonator employed

[SOURCE: IEC 60050-561:2014, 561-03-30, modified – change from crystal oscillator to SAW oscillator and from crystal resonator to SAW resonator.]

3.2.13
voltage controlled SAW oscillator
VCSO
SAW oscillator, the frequency of which can be deviated or modulated according to a specific relation, through application of a control voltage

[SOURCE: IEC 60050-561:2014, 561-03-41, modified – change from crystal resonator to SAW oscillator.]

3.2.14
temperature compensated SAW oscillator
TCSO
SAW oscillator whose frequency deviation due to temperature is reduced by means of a compensation system incorporated in the device

[SOURCE: IEC 60050-561:2014, 561-03-36, modified – change from crystal resonator to SAW oscillator.]

3.2.15
electrostatic micro electro mechanical system oscillator
electrostatic MEMS oscillator
oscillator that uses a MEMS device as the main frequency controlling element

3.2.16
voltage controlled electrostatic MEMS oscillator
electrostatic MEMS oscillator, the frequency of which can be deviated or modulated according to a specified relation, by application of a control voltage

[SOURCE: IEC 60050-561:2014, 561-03-41, modified – change from crystal to MEMS oscillator.]

3.2.17
digital interfaced crystal oscillator
DIXO
crystal oscillator, the frequency and the functions of which can be controlled, by application of an external digital signal

Note 1 to entry: It will be combined as DI-TCXO in TCXO and as DI-OCXO in OCXO.

3.2.18
spread spectrum crystal oscillator
SSXO
crystal oscillator that reduces the peak of frequency spectrum by modulating the oscillation frequency

3.2.19
nominal frequency
frequency given by the manufacturer or the specification to identify the oscillator

[SOURCE: IEC 60050-561:2014, 561-02-31, modified – The word "filter" has been replaced by" oscillator".]

3.2.20
frequency tolerance
maximum permissible deviation of a specified characteristic frequency from the specified value due to a specific cause, or a combination of causes

Note 1 to entry: Frequency tolerances are often assigned separately to specified ambient effects, namely electrical, mechanical and environmental. When this approach is used, it is necessary to define the values of other operating parameters as well as the range of the specified variable, that is to say:

– deviation from the frequency at the specified reference temperature due to operation over the specified temperature range, other conditions remaining constant;

– deviation from the frequency at the specified supply voltage due to supply voltage changes over the specified range, other conditions remaining constant;

– deviation from the initial frequency due to ageing, other conditions remaining constant;

– deviation from the frequency with specified load conditions due to changes in load impedance over the specified range, other conditions remaining constant.

In some cases, an overall frequency tolerance may be specified, due to any/all combinations of operating parameters, during a specified lifetime.

[SOURCE: IEC 60050-561:2014, 561-01-33, modified – Note 1 to entry has been added.]

3.2.21
frequency offset
frequency difference, positive or negative, which should be added to the specified nominal frequency of Oscillator, when adjusting the Oscillator frequency under a particular set of operating conditions in order to minimize its deviation from nominal frequency over the specified range of operating conditions

Note 1 to entry: In order to minimize the frequency deviation from nominal over the entire temperature range, a frequency offset may be specified for adjustment at the reference temperature (see Figure 2).

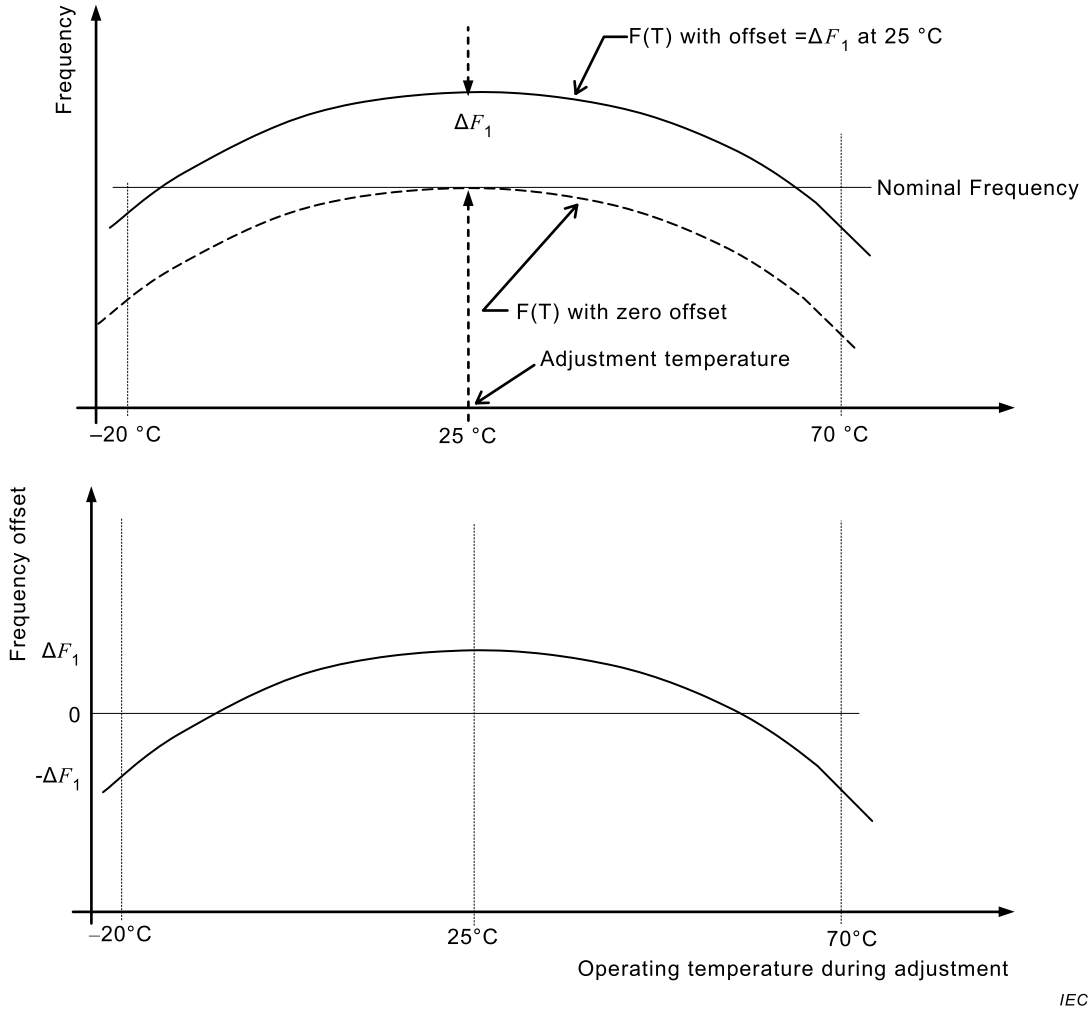


Figure 2 – Example of the use of frequency offset

[SOURCE: IEC 60050-561:2014, 561-03-09]

3.2.22
adjustment frequency
frequency to which an oscillator must be adjusted, under a particular combination of operating conditions, in order to meet the frequency tolerance specification over the specified range of operating conditions

Note 1 to entry: Adjustment frequency corresponds to nominal frequency plus frequency offset.

[SOURCE: IEC 60050-561:2014, 561-03-01]

3.2.23
frequency adjustment range
range over which oscillator frequency may be varied by means of some variable element, for the purpose of

a) setting the frequency to a particular value, or
b) to correct oscillator frequency to a prescribed value after deviation due to ageing, or other changed conditions

Note 1 to entry: For test procedures – see 4.5.11 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-04-1003-07, modified – Note 1 to entry has been added.]

3.2.24
storage temperature range
minimum and maximum temperatures as measured on the enclosure at which an oscillator may be stored without deterioration or damage to its performance

[SOURCE: IEC 60050-561:2014, 561-02-67, modified – The word "the device" has been replaced by "an oscillator".]

3.2.25
operating temperature range, <of an oscillator>
range of temperatures over which the oscillator will function, maintaining frequency and other output signal characteristics within specified tolerances

[SOURCE: IEC 60050-561:2014, 561-03-18]

3.2.26
operable temperature range
range of temperatures over which the oscillator will continue to provide an output signal, though not necessarily within the specified tolerances of frequency, level, waveform, etc.

[SOURCE: IEC 60050-561:2014, 561-01-58, modified – Some elements and specifications have been changed from resonator to Oscillator.]

3.2.27
reference temperature
temperature at which certain Oscillator performance parameters are measured

Note 1 to entry: The reference temperature is normally 25 °C ± 2 °C.

[SOURCE: IEC 60050-561:2014, 561-03-25]

3.2.28
reference point temperature
temperature measured at a specific reference point relative to an oscillator

[SOURCE: IEC 60050-561:2014, 561-03-24]

3.2.29
thermal transient frequency stability
oscillator frequency time response when ambient temperature is changed from one specified temperature to another with a specific rate

[SOURCE: IEC 60050-561:2014, 561-03-37]

3.2.30
stabilization time
duration, measured from the initial application of power, required for an oscillator to stabilize its operation within specified limits

Note 1 to entry: For test procedures – see 4.5.10 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-33, modified – Note 1 to entry has been added.]

3.2.31
frequency/temperature characteristics
deviation from the frequency at the specified reference temperature due to operation over the specified temperature range, other conditions remaining constant

Note 1 to entry: For test procedures – see 4.5.5 of IEC 62884-1:2017.

3.2.32
frequency/temperature stability
maximum permissible deviation of the oscillator frequency, with no reference implied, due to operation over the specified temperature range at nominal supply and load conditions, other conditions constant

$$f - T_{stability} = \pm \frac{(f_{max} - f_{min})}{(f_{max} + f_{min})}$$

where

f_{max} is the maximum frequency measured during the temperature run,

f_{min} is the minimum frequency measured during the temperature run

Note 1 to entry: For test procedures – see 4.5.5 of IEC 62884-1:2017 .

[SOURCE: MIL-PRF-55310E w/Amendment 2:2014]

3.2.33
frequency/voltage coefficient
fractional change in output frequency resulting from an incremental change in supply voltage, other parameters remaining unchanged

Note 1 to entry: In the case of OCXOs, a considerable time may elapse before the full effect of a supply voltage change is observed, as the temperature of the oven may drift gradually to a new value following the voltage perturbation.

Note 2 to entry: For test procedures – see 4.5.7 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-11, modified – Note 2 to entry has been added.]

3.2.34
frequency/load coefficient
fractional change in output frequency resulting from an incremental change in electrical load impedance, other parameters remaining unchanged

Note 1 to entry: For test procedures – see 4.5.6 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-08, modified – Note 1 to entry has been added.]

3.2.35
long-term frequency stability
frequency ageing
relationship between oscillator frequency and time

Note 1 to entry: This long-term frequency drift that is caused by secular changes in the crystal unit and/or other elements of the oscillator circuit, and should be expressed as fractional change in mean frequency per specified time interval.

[SOURCE: IEC 60050-561:2014, 561-03-16]

3.2.36
short-term frequency stability
random fluctuations of the frequency of Oscillator over short periods of time

[SOURCE: IEC 60050-561:2014, 561-03-29]

3.2.37
Allan variance AVAR of fractional frequency fluctuation
AVAR of fractional frequency fluctuation
unbiased estimate of the preferred definition in the time domain of the short-term stability characteristic of Oscillator output frequency:

$$\sigma_y{}^2(\tau) \cong \frac{1}{2(M-1)} \sum_{k=1}^{M-1} (Y_{k+1} - Y_k)^2$$

where

Y_k are the average fractional frequency fluctuations obtained sequentially, with no systematic dead time between measurements;

τ is the sample time over which measurements are averaged;

M is the number of measurements.

Note 1 to entry: The confidence of the estimate improves as M increases.

[SOURCE: IEC 60050-561:2014/AMD1:2016, 561-03-02, modified – The second preferred term has been added.]

3.2.38
Allan deviation of fractional frequency fluctuation
ADEV of fractional frequency fluctuation
measure in the time domain of the short-term frequency stability of Oscillator, based on the statistical properties of a number of frequency measurements, each representing an average of the frequency over the specified sampling interval τ

Note 1 to entry: The preferred measure of fractional frequency fluctuation is:

$$\sigma_y(\tau) \cong \left[\frac{1}{2(M-1)} \sum_{k=1}^{M-1} (Y_{k+1} - Y_k)^2 \right]^{1/2}$$

3.2.39
phase noise
frequency-domain measure of the short-term frequency stability of Oscillator

Note 1 to entry: This phase noise is normally expressed as the power spectral density of the phase fluctuations, $S_\varphi(f)$, where the phase fluctuation function $\phi(t)$ is expressed as;

$$\frac{1}{2\pi} \frac{d\phi(t)}{dt} = F(t) - F_0$$

The spectral density of phase fluctuation can be directly related to the spectral density of frequency fluctuation by

$$S_{\phi}(f) = \left(\frac{F_0}{f}\right)^2 S_y(f) \text{ [rad}^2\text{/Hz]}$$

Where

$F(t)$ is the instantaneous oscillator frequency

F_0 is the average oscillator frequency

f is the Fourier frequency

Note 2 to entry: For test procedures – see 4.5.25 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-22 modified – Note 1 to entry has been modified and Note 2 to entry has been added.]

3.2.40
spectral purity
measure of frequency stability in the frequency domain

Note 1 to entry: This spectral purity is usually represented as the signal side noise power spectrum expressed in decibels relative to total signal power, per hertz bandwidth. This spectral purity includes non-deterministic noise power, harmonic distortion components and spurious single frequency interferences.

Note 2 to entry: For test procedures – see 4.5.29 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-31, modified – Note 2 to entry has been added.]

3.2.41
incidental frequency modulation
optional measure of frequency stability in the frequency domain

Note 1 to entry: Incidental frequency modulation is best described in terms of the spectrum of the resultant base-band signal obtained by applying Oscillator signal to an ideal discriminator circuit of specified characteristics. If the detection bandwidth is adequately specified, the incidental frequency modulation may be expressed as a fractional proportion of the output frequency (for example 2×10^{-8} r.m.s. in a 10 kHz band).

Note 2 to entry: For test procedures – see 4.5.30 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-13, modified – The existing Note 1 and Note 2 have been merged into Note 1 and a new Note 2 to entry has been added.]

3.2.42
amplitude modulation distortion
frequency distortion
amplitude distortion
amplitude/frequency distortion
non-linear distortion in which the relative magnitudes of the spectral components of the modulating signal waveform are modified

Note 1 to entry: For test procedures – see 4.5.22.3 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-03, modified – Note 1 to entry has been added.]

3.2.43
linearity of frequency modulation deviation
measure of the transfer characteristic of a modulation system as compared to an ideal (straight line) function, usually expressed as an allowable non-linearity in per cent of the specified full range deviation

Note 1 to entry: Modulation linearity can also be expressed in terms of the permissible distortion of base-band signals produced by the modulation device (for example, intermodulation and harmonic distortion products shall not exceed –40 dB relative to the total modulating signal power) . For test procedures – see 4.5.23.1 of IEC 62884-1:2017.

Note 2 to entry: Figure 3 is a plot of the output frequency of a typical modulated oscillator specified to have a modulation characteristic of 133,3 Hz/V over a range of ±3 V, with an allowed non-linearity of ±5 %. Curve D is the actual characteristic compared with the ideal (curve A) and the limits (curves B and C).

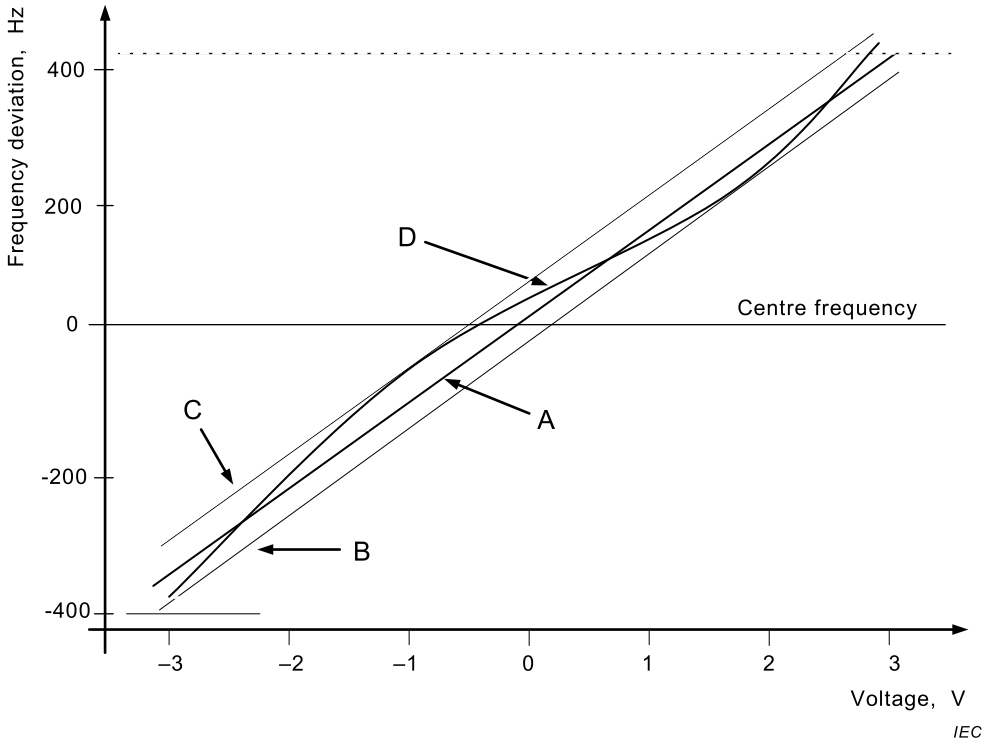


Figure 3 – Linearity of frequency modulation deviation

[SOURCE: IEC 60050-561:2014, 561-03-15, modified – The figure has been modified.]

3.2.44
harmonic distortion
non-linear distortion characterized by the generation of undesired spectral components harmonically related to the desired signal frequency

Note 1 to entry: Each harmonic component is usually expressed as a power ratio (in decibels) relative to the output power of the desired signal.

Note 2 to entry: For test procedures – see 4.5.15 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-12, modified – Note 2 to entry has been added.]

3.2.45
spurious oscillations
discrete frequency spectral components, non-harmonically related to the desired output frequency, appearing at the output terminal of an oscillator

Note 1 to entry: These components can appear as symmetrical sidebands or as signal spectral components, depending upon the mode of generation. Spurious components in the output spectrum are usually expressed as a power ratio (in decibels) with respect to the output signal power.

[SOURCE: IEC 60050-561:2014, 561-03-32]

3.2.46
pulse duration
duration between pulse start time and pulse stop time

SEE: Figure 4.

Note 1 to entry: For test procedures – see 4.5.16.3 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-23, modified – Note 1 to entry has been added.]

3.2.47
rise time
time interval required for the leading edge of a waveform to change between two defined levels

Note 1 to entry: These levels may be two logic levels V_{OL} and V_{OH} or 10 % to 90 % of its maximum amplitude ($V_{HI} - V_{LO}$), or any other ratio defined in the detail specification (see Figure 4)

where

V_{OL} is the low level output voltage;

V_{OH} is the high level output voltage;

V_{HI} is the upper flat voltage of the pulse waveform;

V_{LO} is the low flat voltage of the pulse waveform.

Note 2 to entry: For test procedures – see 4.5.16.2 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-27, modified – Note 2 to entry has been added.]

3.2.48
decay time
fall time
time interval required for the trailing edge of a waveform to change between two defined levels

Note 1 to entry: These levels may be two logic levels V_{OH} and V_{OL} or 90 % to 10 % of its maximum amplitude ($V_{HI} - V_{LO}$), or any other ratio as defined in the detail specification (see Figure 4).

Note 2 to entry: For test procedures – see 4.5.16.2 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-05, modified – The end of the definition has been moved to Note 1 to entry and Note 2 to entry has been added.]

3.2.49
3-state output
output stage which may be enabled or disabled by the application of an input control signal

Note 1 to entry: In the disable mode, the output impedance of the gate is set to a high level permitting the application of test signals to following stages.

Note 2 to entry: For test procedures – see 4.5.21 of IEC 62884-1:2017.

3.2.50
symmetry
mark/space ratio
duty cycle
ratio between the time (t_1), in which the output voltage is above a specified level, and the time (t_2), in which the output voltage is below the specified level

Note 1 to entry: The symmetry is expressed in percent of the duration of the full signal period

Note 2 to entry: The specified level may be the arithmetic mean between levels V_{OL} and V_{OH}, or 50 % of the peak-to-peak amplitude (see Figure 4).

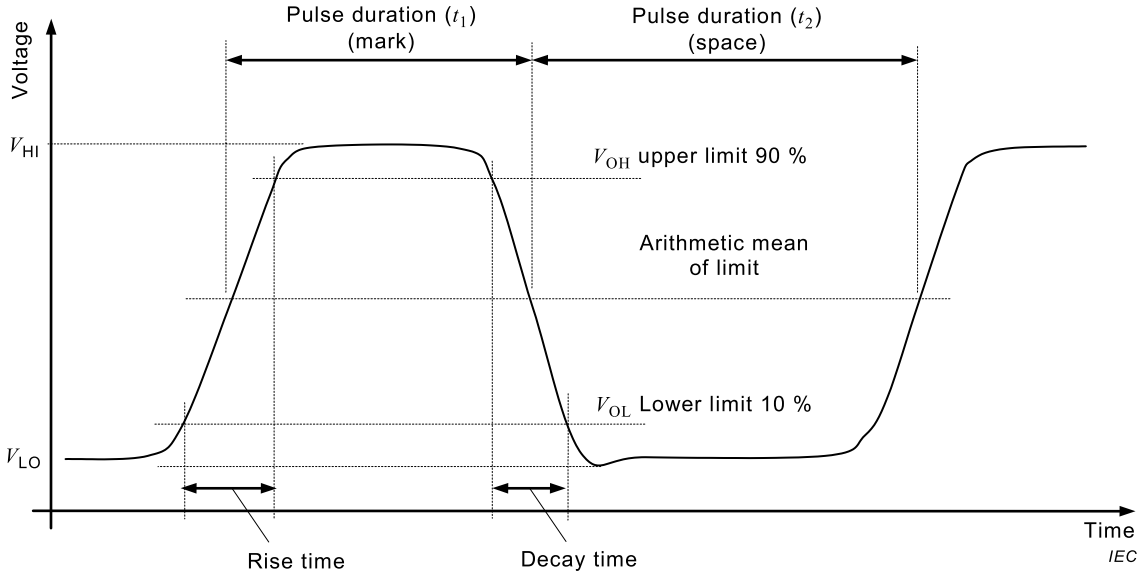


Figure 4 – Characteristics of an output waveform

Note 3 to entry: The ratio is expressed as:

$$\frac{100t_1}{t_1+t_2} : \frac{100t_2}{t_1+t_2}$$

Note 4 to entry: For test procedures – see 4.5.16.4 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-35, modified – In the definition "time period" has been replaced by "time" (twice), the end of Note 2 has been moved to a new Note 3 to entry and a new Note 4 to entry has been added.]

3.2.51
retrace characteristics
ability of oscillator to return, after a specified time period, to a previously stabilized frequency, following a period in the energized condition

Note 1 to entry: For test procedures – see 4.5.12 of IEC 62884-1:2017.

[SOURCE: IEC 60050-561:2014, 561-03-26, modified – Note 1 to entry has been added.]

3.2.52
start-up time
duration t_{SU} between the application of the supply voltage to Oscillator and the time when the r.f. output signal of desired frequency controlled by the quartz resonator fulfils specified conditions:

a) Quasi-sinusoidal waveforms

the signal envelope is 90 % of the steady-state peak-to-peak amplitude (see Figure 5).

b) Pulse waveforms

the output pulse sequence is periodical near the steady-state frequency while its low level V_{LO} remains below V_{OL} and its high level V_{HI} exceeds V_{OH} permanently, where V_{OH} and V_{OL} are defined by the applicable logic family.

Note 1 to entry: The output signal can show spurious oscillations prior to the appearance of the steady-state signal.

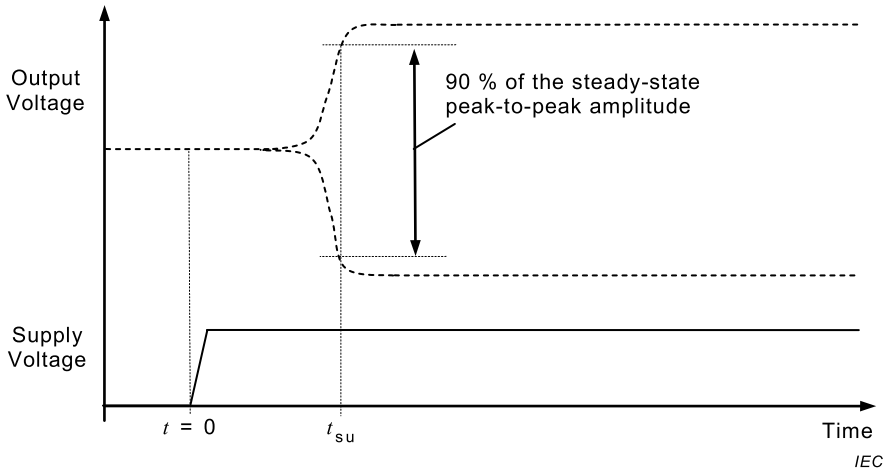


Figure 5 – Definition of start-up time

Note 2 to entry: For test procedures – see 4.5.9 of IEC 62884-1:2017.

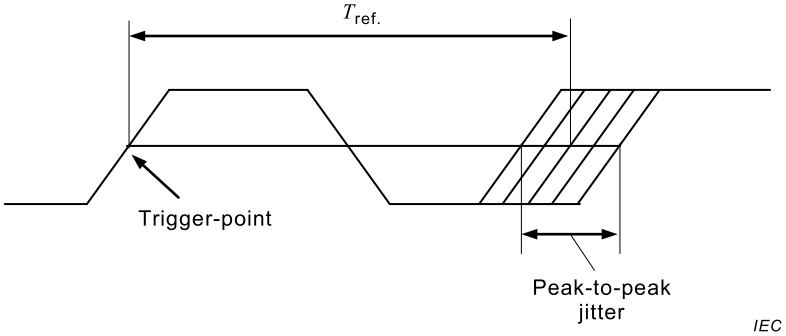
[SOURCE: IEC 60050-561:2014, 561-03-34, modified – Note 1 and Note 2 to entry as well as Figure 5 have been added.]

3.2.53
phase jitter
short-term variation of the zero crossings of the oscillator output signal from their ideal position in time

SEE: Figure 6.

Note 1 to entry: The phase variation Δφ with frequency components greater than or equal to 10 Hz. Variations slower than 10 Hz are called “wander”. Excessive jitter can increase the bit error rate (BER) of a communication signal by incorrectly transmitting a data-stream and can cause synchronization problems.

Note 2 to entry: The corresponding variation of the period length, $\Delta T = \Delta\varphi/(2\pi f_C)$ is called “period jitter” (fc is the clock frequency).



Key

$T_{\text{ref.}}$ is the period of an ideal reference signal.

Figure 6 – Clock signal with period jitter

The jitter amplitude is usually referred to the Unit Interval (UI) of one data bit-width (e.g. UI = 6,43 ns for 155,52 Mbit/s for STM-1/OC-3) or defined as absolute time variation (in nanoseconds, picoseconds or femtoseconds). It is quantified either as the peak-to-peak value, or as the r.m.s. value thereof (see Figure 7).

“Higher confidence levels are required for some applications, so the peak-to-peak jitter can be specified as a larger range of σ in these cases.” See: Figure 6.

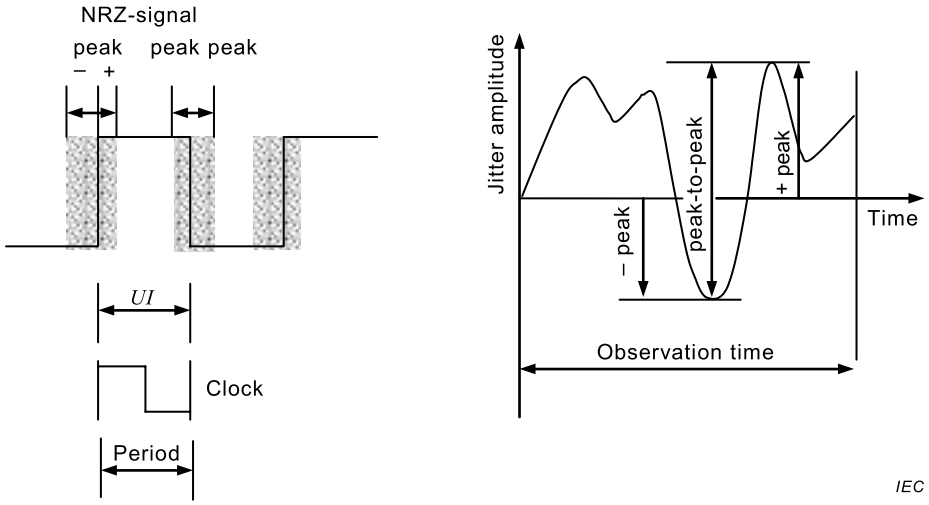


Figure 7 – Phase jitter measures

For random type jitter the r.m.s. value is defined as the standard deviation σ (sigma) of the underlying Gaussian distribution. The peak-to-peak jitter is then the range covered by 7σ (i.e. ±3,5 σ), according to a confidence level of 99,953 48 % (i.e. 465 × 10^{-6} tail). See Figure 8.

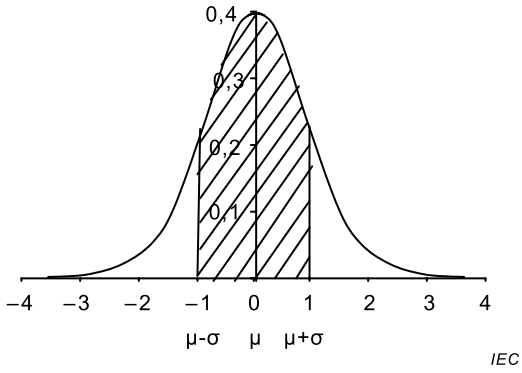


Figure 8 – Gaussian distribution of jitter

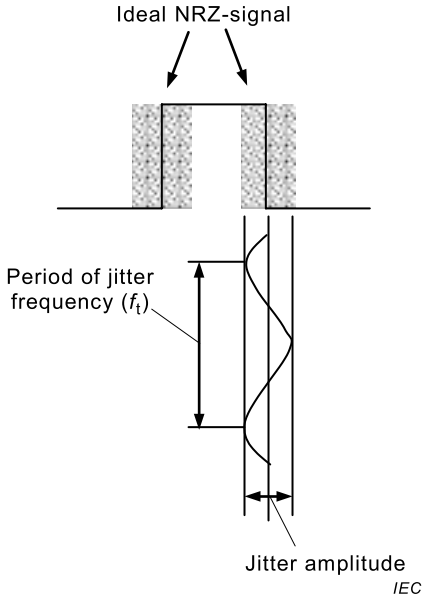


Figure 9 – Jitter amplitude and period of jitter frequency

In the case of subharmonics involved in the signal generation, phase jitter may contain non-random spectral components due to periodical change of the duty cycle. This causes a non-Gaussian distribution, i.e. the 7σ-rule for peak-to-peak values no longer applies. In such cases, only peak-to-peak values are meaningful. However, the determination of peak-to-peak values depends upon observation time. The recommended observation time for peak-to-peak jitter is 1 min. Longer times required when higher confidence is needed (i.e. when a larger range of σ is used to define peak-to-peak random jitter). See Figure 9.

For the characterization of jitter, it is important to define the considered Fourier frequency range, i.e. the frequency components of the jitter itself. This is defined by the application (see standards ITU-T G.825, ATIS-0900101, Telcordia GR-253 and ETSI EN 300 462). See Figure 10.

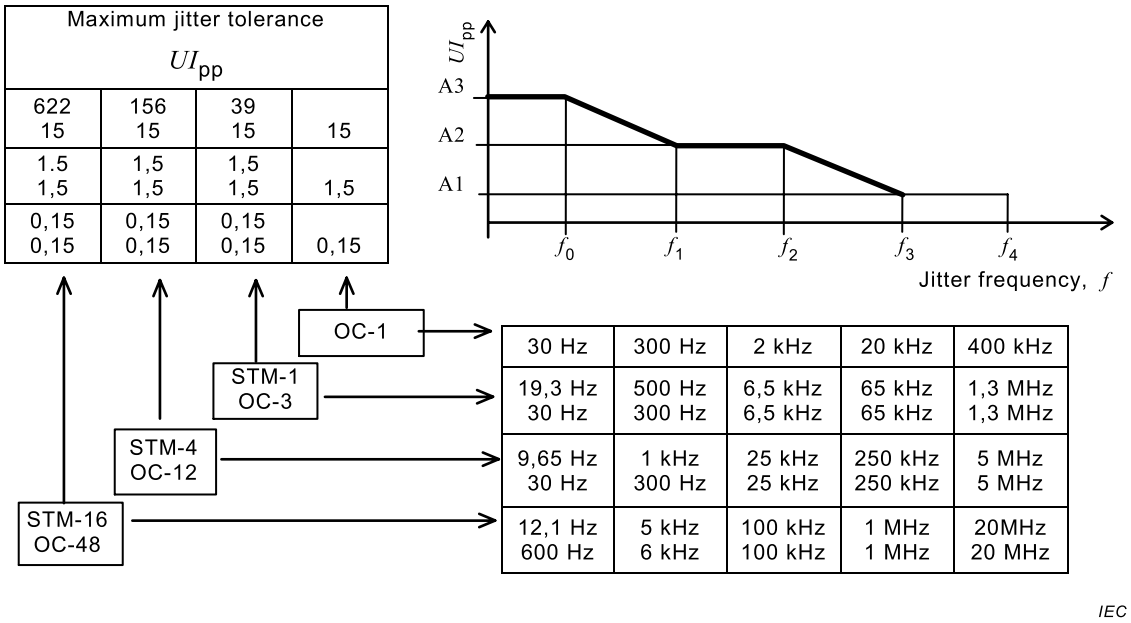


Figure 10 – Jitter tolerance according to ITU-T G.825, ATIS-0900101, Telcordia GR-253 and ETSI EN 300 462

In connection with jitter and wander, the following three parameters are also used for clock characterization:

TIE Time Interval Error (in nanoseconds or picoseconds);

MTIE Maximum Time Interval Error (peak-to-peak TIE);

TDEV Time deviation (r.m.s. value).

TIE is defined as the time deviation between the signal being measured and the reference clock, typically measured in nanoseconds.

MTIE is a measure that characterises frequency offsets. MTIE(τ) is defined as the largest peak-to-peak TIE in any observation interval of length τ (in seconds).

TDEV characterises the spectral content. TDEV(τ) is defined as the r.m.s. of filtered TIE, where the bandpass filter is centered on a frequency of 0,42/τ. It is calculated from the TIE samples for each point τi by the standard deviation σ(τi) (see Note 3).

Note 3 to entry: For more details, refer to standards ITU-T G.810 to G.813, or ATIS-0900101 and ATIS-0900105.03, Telcordia GR-253 and ETSI EN 300462.

[SOURCE: IEC 60050-561:2014, 561-03-21, modified – Note 1 has been expanded and Note 2 and Note3 to entry have been added.]

3.3 Preferred values for ratings and characteristics

3.3.1 General

The values should be preferably chosen from 3.3.2 to 3.3.6, unless otherwise stated in the detail specification.

3.3.2 Climatic category (40/85/56)

For requirements where the operating temperature range of Oscillator is greater than –40 °C to +85 °C, a climatic category consistent with the operating temperature range shall be specified.

3.3.3 Bump severity

The bump severity is (4 000 ± 10) bumps at 400 m/s^2 peak acceleration in each direction along three mutually perpendicular axes. The pulse duration is 6 ms.

NOTE For more details, refer to IEC 60068-2-27.

3.3.4 Vibration severity

The conditions for applying sinusoidal wave vibration severity are the following:

10 Hz to 55 Hz 0,75 mm displacement amplitude (peak value) 55 Hz to 500 Hz or 55 Hz to 2 000 Hz 100 m/s^2 acceleration amplitude (peak value)	30 min in each of three mutually perpendicular axes at 1 octave/min
10 Hz to 55 Hz 1,5 mm displacement amplitude (peak value) 55 Hz to 2 000 Hz 200 m/s^2 acceleration amplitude(peak value)	

NOTE For more details, refer to IEC 60068-2-6.

The conditions for applying random wave vibration severity are the following:

Guidance for suitable levels can be taken from IEC 60068-2-64:2008.

There are two possibilities:

a) chosen from the values given in 5.1 to 5.4 of IEC 60068-2-64:2008;
b) chosen from the examples in Annex A of IEC 60068-2-64:2008 for different environmental conditions.

3.3.5 Shock severity

The shock severity is 1 000 m/s^2 peak acceleration for 6 ms duration; three shocks in each direction along three mutually perpendicular axes, half-sine pulse, unless otherwise stated in the detail specification.

NOTE Refer to IEC 60068-2-27.

3.3.6 Leak rate

- The leak rates are the following: 10^{-1} Pa cm^3/s (10^{-6} bar cm^3/s);
- 10^{-3} Pa cm^3/s (10^{-8} bar cm^3/s).

Refer to IEC 60068-2-17. Match leak rates depending on package volume.

3.4 Marking

3.4.1 General

Oscillator shall be clearly and durably marked with items a) to g) below, and with as many of the remaining items as considered necessary:

a) type designation as defined in the detail specification;
b) nominal frequency in kilohertz or megahertz;
c) year and week of manufacture;
d) mark of conformity (unless a certificate of conformity is used);
e) factory identification code;
f) manufacturer's name or trade mark;
g) terminal identification;
h) designation of electrical connections;
i) power supply voltage and polarity (if applicable);
j) serial number (if applicable).

Where the available surface area of a miniature Oscillator imposes practical limits in the amount of marking, instructions on the marking to be applied shall be given in the detail specification.

3.4.2 Packaging

The primary packaging containing the Oscillator shall be clearly marked with the information listed in 3.4.1 except item g) and electrostatic sensitive device (ESD) identification, where necessary.

4 Quality assessment procedures

4.1 General

Two methods are available for the approval of Oscillator of assessed quality. They are qualification approval and capability approval.

4.2 Primary stage of manufacture

The primary stage of manufacture for Oscillator shall be as follows:

a) for an Oscillator incorporating a resonator:
   – the assembly of the Oscillator;
b) for oscillators incorporating an unencapsulated resonator:
   – the final surface finishing of the element in addition to the assembly of the Oscillator.

4.3 Structurally similar components

The grouping of structurally similar oscillators for the purpose of qualification approval, capability approval and quality conformance inspection shall be prescribed in the relevant sectional specification.

4.4 Subcontracting

There shall be no subcontracting after the assembly of the resonator to the electronic circuit, except in the case of sealed resonator, where the sealing of the final enclosure of the Oscillator may be permitted.

4.5 Incorporated components

Where the final component contains components of a kind covered by a generic specification in the IEC series, these shall be produced using the normal IEC release procedures.

Where the contained components are not produced to an IEC detail specification, the approved manufacturer's chief inspector shall verify their quality by the use of

- a procurement specification covering all aspects necessary to ensure their satisfactory performance as part of the final product;
- an adequate approval test program maintaining a record of results;
- sufficient goods inward inspection procedures to ensure continued satisfactory performance of the final product.

4.6 Manufacturer’s approval

To obtain manufacturer's approval, the manufacturer shall be accredited by the maintenance of quality by the third-party certification body, or shall be guaranteed the quality by mutual authentication between the manufacturer and the user.

4.7 Approval procedures

4.7.1 General

To qualify an Oscillator, either capability approval or qualification approval procedures may be used.

4.7.2 Capability approval

Capability approval is appropriate when structurally similar oscillators based on common design rules, are fabricated by a group of common processes.

Under capability approval, detail specifications fall into the following three categories:

a) capability qualifying components (CQCs)

   A detail specification shall be prepared for each CQC as agreed with the NSI. It shall identify the purpose of the CQC and include all relevant stress levels and test limits;

b) standard catalogue items

   When a component covered by the capability approval procedure is intended to be offered as a standard catalogue item, a detail specification complying with the blank detail specification shall be written.

c) custom built Oscillator

   The contents of the detail specification shall be by agreement between the manufacturer and the customer.

Further information on detail specifications is contained in the sectional specification IEC 60679-4.

The product and capability qualifying components (CQCs) are tested in combination and approval given to a manufacturing facility on the basis of validated design rules, processes and quality control procedures. Further information is given in 4.8 and in the sectional specification IEC 60679-4.

4.7.3 Qualification approval

Qualification approval is appropriate for components manufactured to a standard design and established production process and conforming to a published detail specification.

The program of tests defined in the detail specification for the appropriate assessment and severity level applies directly to the Oscillator to be qualified, as required in 4.9 and the sectional specification IEC 60679-5.

4.8 Procedures for capability approval

4.8.1 General

The procedures for capability approval shall be based on the method according to the certification body to certify the maintenance of quality.

4.8.2 Eligibility for capability approval

The manufacturer shall comply with the primary stage of manufacture as defined in 4.2 of this generic specification.

4.8.3 Application for capability approval

The application for capability approval shall be based on the method according to the certification body to certify the maintenance of quality.

4.8.4 Granting of capability approval

A certification is granted to an organization (manufacturer) when it has been established that their capability for manufacturing processes and quality control methods (including design aspects as applicable) covering a specific component technology, fulfils the requirements of the relevant specification or standard.

4.8.5 Capability manual

The contents of the capability manual shall be in accordance with the requirements of the sectional specification.

The NSI shall treat the capability manual as a confidential document. The manufacturer may, if he so wishes, disclose part or all of it to a third party.

4.9 Procedures for qualification approval

4.9.1 General

The procedures for qualification approval shall be based on the method according to the certification body to certify the maintenance of quality.

4.9.2 Eligibility for qualification approval

The manufacturer shall comply with the primary stage of manufacture as defined in 4.2 of this generic specification.

4.9.3 Application for qualification approval

The application for qualification approval shall be based on the method according to the certification body to certify the maintenance of quality.

4.9.4 Granting of qualification approval

Qualification approval shall be granted when the procedures are in accordance with 4.8.4 of this generic specification.

4.9.5 Quality conformance inspection

The blank detail specification associated with the sectional specification shall prescribe the test schedule for quality conformance inspection.

4.10 Test procedures

The test procedures to be used shall be selected from IEC 62884-1:2017. If any required test is not included, then it shall be defined in the detail specification.

4.11 Screening requirements

Where screening is required by the customer for an Oscillator, this shall be specified in the detail specification.

4.12 Rework and repair work

4.12.1 Rework

Rework is the rectification of processing errors and shall not be carried out if prohibited by the sectional specification. The sectional specification shall state if there is a restriction on the number of occasions that rework may take place on a specific component.

All rework shall be carried out prior to the formation of the inspection lot offered for inspection to the requirements of the detail specification.

Such rework procedures shall be fully described in the relevant documentation produced by the manufacturer and shall be carried out under the direct control of the chief inspector.

Subcontracting of rework is not permitted.

4.12.2 Repair work

Repair work is the correction of defects in a component after release to the customer.

Components that have been repaired can no longer be considered as representative of the manufacturer's production.

4.13 Certified test records

When certified test records (CTR) are prescribed in the sectional specification for qualification approval and are requested by the customer, the results of the specified tests shall be summarized.

4.14 Validity of release

An Oscillator held for a period exceeding two years following acceptance inspection shall be reinspected for the electrical tests, prior to release.

4.15 Release for delivery

Release for delivery is valid for five years unless a shorter period is specified in the detail specification or standard. The relevant specification or standard shall prescribe the tests that shall be repeated in order to revalidate the release.

4.16 Unchecked parameters

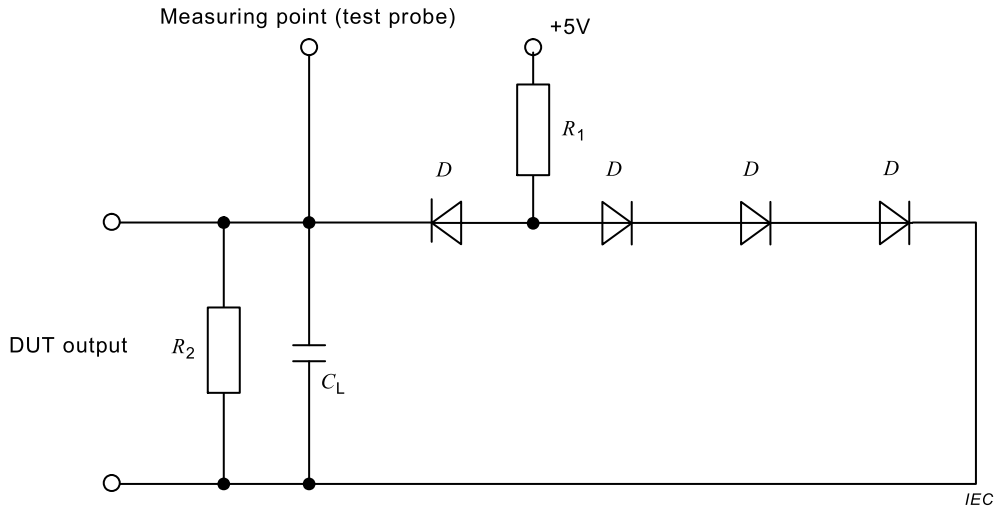
Only those parameters of a component which have been specified in a detail specification and which were subject to testing, can be assumed to be within the specified limits. It should not be assumed that any parameter not specified will remain unchanged from one component to another. Should it be necessary for further parameters to be controlled, then a new, more extensive, detail specification should be used. The additional test method(s) shall be fully described and appropriate limits, AQLs and inspection levels specified.

Annex A
(normative)

Load circuit for logic drive

A.1 TTL and Schottky

The test fixture for an Oscillator designed with logic drive circuits shall simulate the load conditions which the Oscillator is required to drive. Preferred test circuits for TTL and Schottky logic are shown in Figures A.1 and A.2, respectively.



– diodes marked D shall be type 1N916 or 1N3064;

– diodes marked D_S shall be high speed Schottky type;

– values for R_1 and R_2 are dependent on the load requirement and may be calculated using the formulae:

$$R_1 = \frac{5 - (V_{OL} + V_D)}{n|I_{IL}|}$$

$$R_2 = \frac{V_{OH}}{n|I_{IH}|}$$

where

n is the number of gates;

V_{OL} is the Oscillator low level output voltage;

I_{IL} is the low level input current per gate;

V_{OH} is the Oscillator high level output voltage;

I_{IH} is the high level input current per gate;

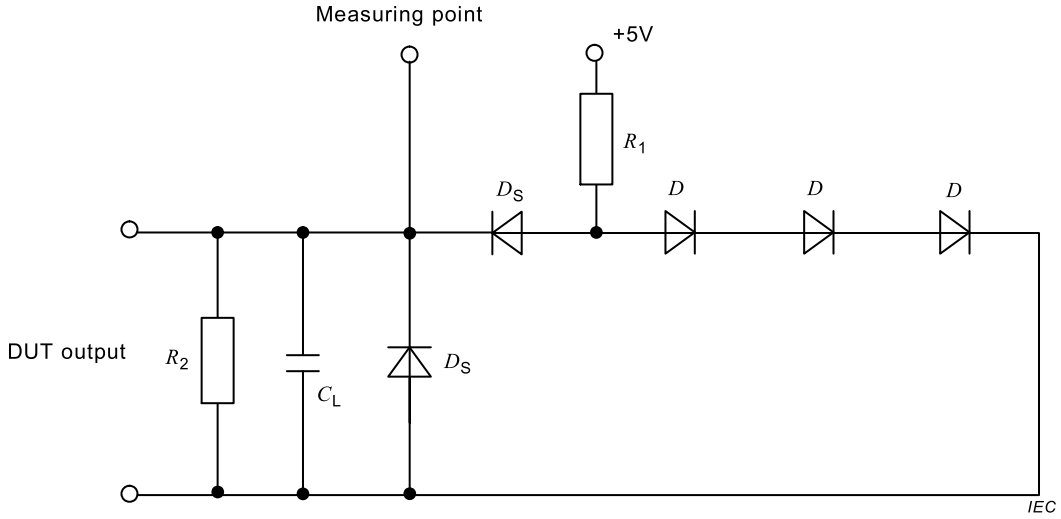
V_D is the voltage drop across the diode.

NOTE 1 Standard TTL (54/74 series)

High speed TTL (54/74 series)

NOTE 2 V_D = 0,65 V

Figure A.1 – Circuit for TTL



– diodes marked D shall be type 1N916 or 1N3064;

– diodes marked D_S shall be high speed Schottky type;

– values for R_1 and R_2 are dependent on the load requirement and may be calculated using the formulae:

$$R_1 = \frac{5 - (V_{OL} + V_D)}{n|I_{IL}|}$$

$$R_2 = \frac{V_{OH}}{n|I_{IH}|}$$

where

n is the number of gates;

V_{OL} is the Oscillator low level output voltage;

I_{IL} is the low level input current per gate;

V_{OH} is the Oscillator high level output voltage;

I_{IH} is the high level input current per gate;

V_D is the voltage drop across the diode.

NOTE 1 Schottky logic (54S/74S series)

Low power Schottky logic (54LS/74LS Series)

NOTE 2 V_D = 0,45 V

Figure A.2 – Circuit for Schottky logic

Values of these parameters for various TTL series for use in the above formulae are given in Table A.1.

Values for C_L are also given. It should be noted that C_L includes the probe and fixture capacitance.

The Oscillator output voltage limit requirements using the test circuits of Figures A.1 and A.2 will normally be:

V_{OH} = 2,4 V min.

V_{OL} = 0,5 V max.

Table A.1 – Values to be used when calculating R_1 and R_2

TTL Series	74	54	74H	54H	74L	54L	74LS	54LS	74S	54S
V_{OH} (V)	2,4	2,4	2,4	2,4	2,4	2,4	2,7	2,7	2,7	2,7
V_{OL} (V)	0,4	0,4	0,4	0,4	0,3	0,3	0,4	0,4	0,5	0,5
I_{IH} (µA)	40	40	50	50	10	10	20	20	50	50
I_{IL} (mA)	–1,6	–1,6	–2,0	–2,0	–0,18	–0,18	–0,4	–0,4	–2,0	–2,0
C_L (pF)	15	15	25	25	50	50	15	15	15	15

The following information shall be specified in the detail specification:

R_1, R_2, C_L, V_{OH} and V_{OL}, together with the circuits to which reference is made.

Satisfactory operation in a particular circuit should not be considered as an assurance that a specific oscillator will operate satisfactorily with all types of TTL logic.

A.2 CMOS

The test fixture for an Oscillator designed for CMOS logic circuits should simulate the load conditions which the Oscillator is required to drive. The load circuit shall consist of a capacitance which shall be 10 pF times the number of gates being driven. The figure of 10 pF includes a 2,5 pF allowance for strays.

Satisfactory operation under these conditions should not be considered as an assurance that a specific Oscillator will operate in a satisfactory manner in any CMOS logic circuit.

A.3 ECL

The test fixture for an Oscillator designed with logic drive circuits shall simulate the load conditions which the Oscillator is required to drive. Preferred test circuits for ECL logic are shown in Figure A.3. The load circuits shall consist of a resistance which shall be 50 Ω to V_{CC} –2 V. Operating condition and DC electrical characteristics for various ECL series for use are given in Table A.2 and Table A.3.

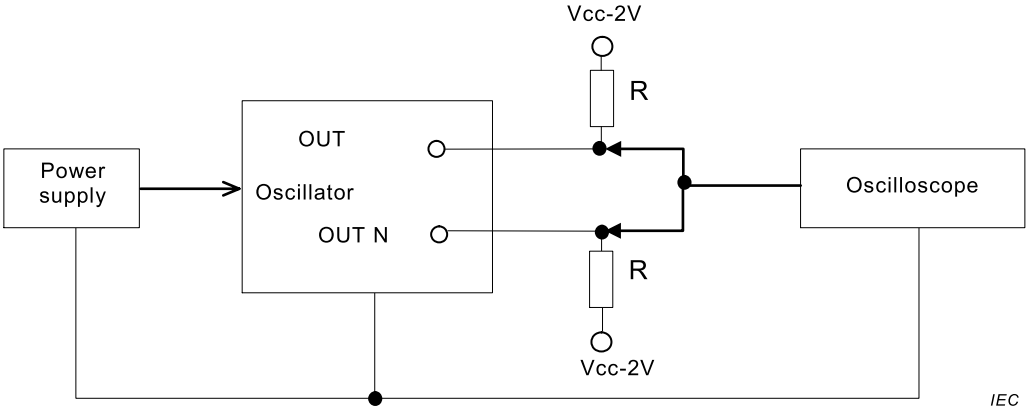


Figure A.3 – Circuit for PECL

Table A.2 – Operating condition

ECL Series	300K ECL	101K ECL	PECL	LVPECL	LVPECL
V_{CC}(V)	0	0	5,0	3,3	2,5
V_{EE}(V)	-3,5	-5,2	0	0	0

Table A.3 – DC Electrical characteristics output load = 50 Ω to Vcc-2V

PARAMETER	SYMBOL	MIN	MAX
Output HIGH Voltage (mV)	V_{OH}	Vcc-1 025	Vcc-880
Output LOW Voltage (mV)	V_{OL}	Vcc-1 810	Vcc-1 620
Output reference Voltage (mV)	V_{BB}	Vcc-1 380	Vcc-1 260

A.4 LVDS

The test fixture for an Oscillator designed with logic drive circuits shall simulate the load conditions which the Oscillator is required to drive. Preferred test circuits for LVDS logic are shown in Figure A.4. The load circuits shall consist of a resistance which shall be 100 Ω between each output port.

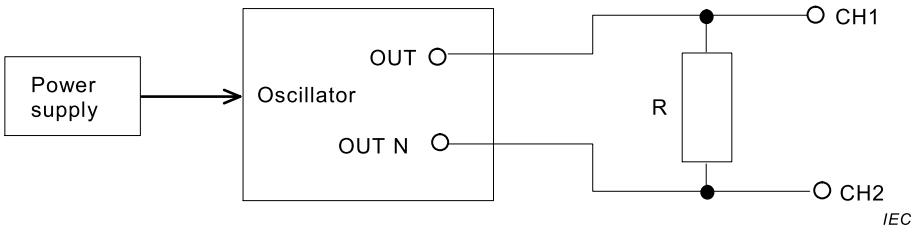


Figure A.4 – Circuit for LVDS

The Oscillator output requirements result in a balanced source that will produce a differential voltage across a test termination load of 100 Ω in the range of 250 mV to 450 mV. The steady-state magnitude of the Oscillator output offset voltage measured between the centre point of the test load and the Oscillator output common shall be greater than or equal to 1,125 V and less than or equal to 1,375 V.

Annex B
(normative)

Latch-up test

B.1 Definition

B.1.1 Latch-up

Latch-up is a state in which a low-impedance path results from (and persists following) an input, output or supply overvoltage.

B.1.2 Test procedure

The latch-up test under static conditions subjects a device to greater stresses than it would encounter in normal operation and is even more severe than dynamic test methods using similar levels of current and voltage.

This test, if performed according to the procedures defined in this document, is a necessary and sufficient method for the characterization of the latch-up susceptibility or immunity of an Oscillator incorporating CMOS integrated circuits.

B.2 Test method

The following applies as regards the test method:

- This test is destructive.
- This test is applicable only to oscillators containing CMOS integrated circuits.
- This test shall be performed in accordance with IEC 60748-2.
- This test is a recommended test procedure. It is not a specification. No test limits are given.
- This test is performed for characterization and inspection purposes only. It is not a production test.

Annex C
(normative)

Electrostatic discharge sensitivity classification

C.1 Definition

C.1.1 Electrostatic discharge (ESD)

Electrostatic discharge is a transfer of electric charge between bodies of different electrostatic potentials in proximity or through direct contact.

C.1.2 Test procedure

This method establishes the procedure for classifying oscillators, built with CMOS ICs, according to their susceptibility or immunity to damage or degradation caused by exposure to electrostatic discharge (ESD). This classification is used to specify appropriate packaging and handling requirements to provide classification data.

C.2 Test methods

C.2.1 General

This test is destructive.

C.2.2 Leaded oscillator

For oscillators intended in manual assembly specification according by the Human Body Model (HBM).

The test procedure as defined in IEC 61340-5-1, IEC TR 61000-4-1 and IEC 60749-26 applies.

If not otherwise specified, the recommended test voltage is maximum 2 000 V.

Another maximum test voltage may be negotiated between manufacturer and customer.

C.2.3 SMD oscillator

Since these oscillators are usually assembled onto printed wiring boards (PWBs) by automated processes, the Machine Model (MM) shall be applied.

The test procedure as defined in IEC 61340-5-1, IEC TR 61000-4-1 and IEC 60749-27 applies.

If not otherwise specified, the recommended test voltage is maximum 200 V.

Another maximum test voltage may be negotiated between manufacturer and customer.

C.2.4 The impact of ESD on Oscillator in steady-state

Certain applications require that the output of the Oscillator shall not be disrupted, even for a single cycle, if the Oscillator enclosure is subjected to an ESD pulse.

A suitable test method is under consideration.

Annex D
(normative)

Digital interfaced crystal oscillator's function

DIXO is accessed by using a digital communication channels in a register that is incorporated in, it is possible to control the frequency and output level of the oscillator and the condition monitoring.

In addition to the functions performed by the digital interface (see Table D.1), it can assign any function not limited to monitoring and control.

Table D.1 – Function of the digital interface

Function	Content
Frequency control value	Frequency control data
Status information	Status information indicating the operating status (Such as in the case of oven alarm information at OCXO)
Reservation	Reservation is an area that can be used to specify a manufacturer, does not specify the content and function

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